IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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|---|---|---|---|
| First Named Inventor | : | Baowei KANG | |
| Appln. No. | : | 10/017,734 | |
| Filed | : | December 18, 2001 | Group Art Unit: 2823 |
| Title | : | POWER SEMICONDUCTOR SWITCHING DEVICES WITH LOW POWER LOSS AND METHOD FOR FABRICATING THE SAME | Examiner: Khiem D. Nguyen |
| Docket No. | : | B784.312-1 | |

# RESPONSE

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**SENT VIA EXPRESS MAIL**

Express Mail No.: EV 331789706 US

Sir:

This Response is submitted with a Request for Continuing Examination (RCE), and is in response to the Advisory Action mailed March 4, 2004, in which claims 2-6 and 8-14 were pending. In the Advisory Action, claims 2-6 and 8-14 were rejected under 35 U.S.C. §103(a) as being unpatentable over Francis et al. (U.S. Patent No. 6,482,681). It is respectfully submitted that all of pending claims 2-6 and 8-14 are in condition for allowance. Reconsideration and notice to that effect is respectfully requested.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. MPEP 2143.03; *In re Royka*, 490 F.2d 981 (CCPA 1974). As discussed in section I below, independent claims 6 and 9 require fabricating a device including a diffused $n^+$ buffer layer formed on a backside of the wafer, which is not disclosed, taught or suggested by the cited prior art (Francis et al.). Rather, Francis et al. teach the formation of the $n^+$ buffer layer via hydrogen implantation. In addition, *prima facie* obviousness can only be established by modifying a prior art reference when there is some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the

art, to modify the reference. MPEP 2143.01; *In re Kotzab*, 217 F.3d 1365 (Fed. Cir. 2000). In this case, the Examiner contended that it would have been obvious to modify the teachings of Francis et al. to (a) perform the step of forming the $n^+$ buffer layer by diffusion rather than by hydrogen implantation as taught, and to (b) perform the step of diffusing the $N^+$ layer on the backside of the wafer in the first step rather than in the last or next-to-last step as taught. A particular claimed order of performing the steps of a process can be shown to be nonobvious if new or unexpected results are achieved. See *In re Burhans*, 154 F.2d 690 (CCPA 1946). As discussed in section II below, the order of the fabrication steps for the low power loss semiconductor switching device of the present invention (forming a diffused $n^+$ layer on the backside of the wafer in the first step, as recited in independent claims 6 and 9) produces new and superior results over the cited prior art (Francis et al.), and is therefore a nonobvious distinction over the prior art.

I. Francis et al. do not disclose, teach or suggest forming a *diffused* $n^+$ layer

Independent claims 6 and 9 require fabricating a device including a diffused $n^+$ buffer layer formed on a backside of the wafer. Francis et al. fail to show, teach, or suggest forming a diffused $n^+$ buffer layer on a backside of the wafer. Rather, Francis et al. teach the formation of the $n^+$ buffer layer via hydrogen implantation.

A diffused $n^+$ buffer layer provides several advantages over an $n^+$ buffer layer formed via hydrogen implantation. First, the diffusion of the $n^+$ buffer layer can be performed on many wafers at the same time, while hydrogen implantation must be performed on each individual wafer. Hydrogen implantation thus reduces productivity and increases fabrication costs compared to diffusion. Furthermore, hydrogen implantation typically has a lower ion beam current (or flux) than that of other n-type dopant ion implantations such as P or As, which further slows down production.

Diffusion of the $n^+$ buffer layer according to the procedure of the present invention also provides high controllability of the fabrication process. In particular, the diffusion of the $n^+$ buffer layer according to the procedure of the present invention introduces one main shallow donor, which provides a controllable doping concentration. On the other hand, hydrogen implantation in silicon combined with low temperature annealing (300-500°C), as taught by Francis et al., is not as controllable. Hydrogen implantation (or proton irradiation), combined with low temperature

annealing, provides hydrogen-related shallow donors, which produces n-type doping in the buffer layer. However, it has been shown that *three* shallow level distributions are introduced during hydrogen implantation in silicon during low temperature annealing. *Mat. Sci. Eng.*, B58 108-112 (1999). Furthermore, when the fluence (or dose) of hydrogen ions is increased to greater than or equal to $5\times10^{12}$ $cm^{-2}$, only two shallow level distributions are clearly shown. *IEEE Trans. Nucl. Sci.*, Vol. 41, No. 6, 1932-1936 (1994). Accordingly, different doses of hydrogen ions produce a different number of donor levels, resulting in unexpected doping concentrations. Also, the defects which act as shallow donors in hydrogen-implanted silicon can compromise the original doping concentration of the buffer layer. *Id.* Thus, hydrogen implantation combined with low temperature annealing is a less controllable and reliable procedure than the procedure of the present invention.

Finally, it has been found that defects which act as shallow donors in hydrogen-implanted silicon can change reversibly. *Nucl. Inst. Meth.*, 209/210 (1983) 677-682. More specifically, when the device temperature changes from more than 300°C (annealing temperature) to lower than 100°C (common operating temperature of power devices), the equilibrium concentration of shallow donors (or, doping concentration of the n-type buffer layer) decreases, and vice versa. The variation with temperature of the equilibrium concentration of shallow donors means that the n-type doping of the buffer layer is not stable in a temperature-varying situation (which is common for power devices). All of these effects of hydrogen implantation combined detrimentally affect the controllability of the fabricating process and the performance stability and reliability of the IGBT as a power device.

There is some disclosure in the Francis et al. patent that a "punch-through IGBT can also [be] created using a diffused wafer." Column 5, lines 47-48. However, this disclosure is characterized as "difficult if not impossible to control" (column 5, lines 65) and would therefore teach one skilled in the art <u>not</u> to use a diffused wafer, but instead use a hydrogen implanted wafer, as explicitly set forth at column 6, lines 3-6.

The above evidence of new and superior results of the claimed diffused $n^+$ layer over the hydrogen implanted layer taught by the prior art shows that the teachings of the prior art are highly dissimilar to the claimed invention, and that it therefore would not have been obvious to

modify the hydrogen implantation teachings of the prior art without an explicit suggestion or motivation to do so. Such a suggestion or motivation has not been found, either in the Francis et al. patent or elsewhere in the prior art (the only suggestion in the Francis et al. patent actually teaches away from such a modification). As such, the rejection of independent claims 6 and 9 under 35 U.S.C. § 103 should be withdrawn.

II. The claimed order of steps produces new and superior results to Francis et al.

Independent claims 6 and 9 require fabricating from a uniformly-doped monocrystalline $n^-$ starting wafer a nonuniformly doped n-type substrate which contains an $n^-$ layer on a frontside of the wafer and a diffused $n^+$ layer on a backside of the wafer, wherein the diffused $n^+$ layer is formed in the first step. The diffused layer is formed in the first step of this procedure by heavily diffusing certain n-type dopants into both sides of an $n^-$ substrate at the same time. One (on the final frontside) of the two diffused layers is then removed by grinding, and the exposed surface of the $n^-$ substrate is further ground and polished to a proper position according to the required voltage rating of the device, thus the nonuniformly-doped substrate containing a diffused $n^+$ layer (on the final backside) is achieved. As is well known, the doping concentration decays from the backside to the frontside.

Francis et al. teach the formation of an insulated gate bipolar transistor (IGBT) including an $n^+$ buffer layer and a weak backside emitter formed on an $n^-$ monocrystalline (normally FZ) wafer (i.e., non-epi). In particular, Francis et al. teach that a diffused wafer can be used to create a punch-through IGBT, with the $n^+$ buffer being diffused *just prior* to complete backside thinning of the wafer. *See* col. 5, lines 51-55. This step is performed *after* the frontside structure of the wafer has been formed. According to Francis et al., the formation of the IGBT device, and in particular the intersection of the $P^+$ region and the $N^+$ gradient curve, using present day equipment, is too variable to precisely control the forward voltage drop ($V_{ce}$) and speed of the device. This problem is solved, according to Francis et al., by forming the $n^+$ buffer layer via implantation of hydrogen ions in the bottom of the thinned wafer to control the concentration of the $n^+$ buffer at the bottom surface. The implantation of hydrogen ions is performed after thinning of the backside of the wafer.

The diffusion of the $n^+$ buffer layer in the first step according to the process of the present invention provides several new and superior advantages over the IGBT fabrication taught by Francis et al. First, in the fabrication sequence taught by Francis et al., the backside $n^+$ diffusion must be carried out at a high temperature (more than 1000 °C) for a prolonged period of time (from several tens of minutes to several hours or more, depending on the starting and thinned thicknesses of the wafer). Forming the $n^+$ buffer layer *after* fabrication of the frontside structure and/or after thinning of the backside of the wafer, as is taught by Francis et al., is likely to destroy the frontside structure during the high temperature process of the backside $n^+$ diffusion. For example, the high temperature process may affect various frontside structures such as the junction depths of the $p^+$ body (or $p^+$ well) and the $n^-$ source region, the channel length, the integrity of the contacts between the silicon and the electrode metal, and the integrity of the top surface passivation layers. In contrast, by fabricating the diffused $n^+$ layer in the first step, as is done in the fabrication process of the present invention, adverse effects which may occur to the frontside structure during high temperature processes are avoided. Therefore, the fabrication steps for the low power loss semiconductor switching device of the present invention produces new and superior results over Francis et al.

Therefore, because the order of fabrication steps for the low power loss semiconductor switching device of the present invention produces new and superior results over Francis et al., and Francis et al. does not show, teach, or suggest forming a low power loss semiconductor switching device including a diffused $n^+$ layer on a backside of the wafer, the rejections to independent claims 6 and 9 under 35 U.S.C. § 103(a) should accordingly be withdrawn.

Claims 2-5, 8, and 10-14 were also rejected under 35 U.S.C. § 103(a) as being anticipated by Francis et al. As discussed above, claims 6 and 9 are now in a condition for allowance. Claims 2-5 and 8 depend from allowable claim 6 and claims 10-13 depend from allowable claim 9. These claims are also allowable, since any claim depending from a patentable independent claim is also patentable. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

## CONCLUSION

In view of the foregoing, all pending claims 2-6 and 8-14 are in condition for allowance. Reconsideration and allowance of all pending claims are respectfully requested.

Respectfully submitted,

KINNEY & LANGE, P.A.

Date: 3/30/04

By _____

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AMK/PGK

# FEE TRANSMITTAL


Total Amount of Payment $860.00

| Complete if Known | |
|---|---|
| Application No. | 10/017,734 |
| Filing Date | December 18, 2001 |
| First Named Inventor | Baowei KANG |
| Group Art Unit | 2823 |
| Examiner Name | Khiem D. Nguyen |
| Atty. Docket Number | B784.312-1 |

## METHOD OF PAYMENT (Check One)

1. [X] The Commissioner is hereby authorized to charge any additional fee required under 37 C.F.R. 1.16 and 1.17 and credit any over payments to Deposit Account No.11-0982. Deposit Account Name: Kinney & Lange, P.A. A duplicate copy of this communication is enclosed

2. [X] Check Enclosed

## FEE CALCULATION

### 1. BASIC FILING FEE

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description |
|---|---|---|---|---|
| 1001 | 770 | 2001 | 385 | [ ] Utility Filing Fee |
| 1002 | 340 | 2002 | 170 | [ ] Design Filing Fee |
| 1004 | 770 | 2004 | 385 | [ ] Reissue Filing Fee |
| 1005 | 160 | 2005 | 80 | [ ] Prov. Filing Fee |

Subtotal (1) $-0-

### 2. EXTRA CLAIM FEES

| | Number Claims | Prior | Extra | Fee from Below | Fee Paid |
|---|---|---|---|---|---|
| Total | __ - | __ = | __ X | __ = | __ |
| Indep. | __ - | __ = | __ X | __ = | __ |
| Multiple Dependent Claims | | | | __ = | __ |

Insert 3 and 20, or number previously paid if greater; Reissue see below

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Description |
|---|---|---|---|---|
| 1202 | 18 | 2202 | 9 | Claims in excess of 20 |
| 1201 | 86 | 2201 | 43 | Independent claims in excess of 3 |
| 1203 | 290 | 2203 | 145 | Multiple Dependent Claim |
| 1204 | 86 | 2204 | 43 | Reissue Independent Claims Over Original Patent |
| 1205 | 18 | 2205 | 9 | Reissue claims in excess of 20 and over original patent |

Subtotal (2) $-0-

## FEE CALCULATION (Continued)

### 3. ADDITIONAL FEES

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee paid |
|---|---|---|---|---|---|
| 1051 | 130 | 2051 | 65 | Surcharge - Late filing fee or oath | __ |
| 1052 | 50 | 2052 | 25 | Surcharge - late provisional filing fee or cover sheet | __ |
| 1053 | 130 | 1053 | 130 | Non-English specification | __ |
| 1812 | 2,520 | 1812 | 2,520 | For Filing a Request for Reexamination | __ |
| 1251 | 110 | 2251 | 55 | Extension for reply within first month | __ |
| 1252 | 420 | 2252 | 210 | Extension for reply within second month | __ |
| 1253 | 950 | 2253 | 475 | Extension for reply within third month | 475 |
| 1254 | 1,480 | 2254 | 740 | Extension for reply within fourth month | __ |
| 1255 | 2,010 | 2255 | 1,005 | Extension for reply within fifth month | __ |
| 1402 | 330 | 2402 | 165 | Filing a brief in support of an appeal | __ |
| 1403 | 290 | 2403 | 145 | Request for oral hearing | __ |
| 1814 | 110 | 2814 | 55 | Terminal Disclaimer Fee | __ |
| 1452 | 110 | 2452 | 55 | Petition to revive - unavoidable | __ |
| 1453 | 1,330 | 2453 | 665 | Petition to revive - unintentional | __ |
| 1501 | 1,330 | 2501 | 665 | Utility/Reissue issue fee | __ |
| 1502 | 480 | 2502 | 240 | Design issue fee | __ |
| 1460 | 130 | 1460 | 130 | Petitions to the Commissioner | __ |
| 1807 | 50 | 1807 | 50 | Petitions related to provisional applications | __ |
| 1806 | 180 | 1806 | 180 | Submission of Information Disclosure Statement | - |
| 8021 | 40 | 8021 | 40 | Recording each patent assignment per property (times number of properties) | __ |
| 1801 | 770 | 2801 | 385 | Request for Continued Examination (RCE) | 385 |

Other fee (specify) _____ __

Subtotal (3) $860.00

Signature _____ Reg. No. 43,724

Alan M. Koenck

Date March 30, 2004 Deposit Account No. 11-0982